The output signal, SGNOUT, (output 18) is fed to the ADC. The voltage range of SGNOUT is 1.5V...3.5V. The intermediate level of SGNOUT is derived from the VREF voltage level, which is made by the ADC.

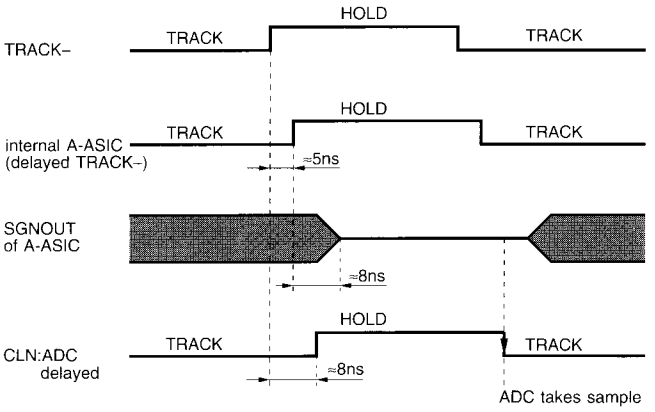


Figure 3.13 Track & Hold timing

External Trigger Amplifier

This amplifier section processes the incoming external trigger signal so that it can be used in the trigger section. The input of this section is TTL compatible.

Trigger Selector

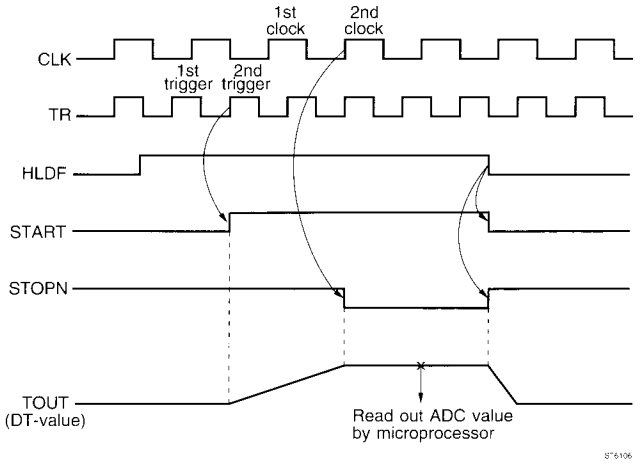
In this section the channel A, channel B or external trigger input signal is selected to act as trigger source. The trigger slope is also selected in this block.

Hysteresis

The hysteresis section converts the trigger signal into a pulse shaped signal. Because of the hysteresis, the circuit will not trigger on noisy signals. The LEVEL signal (input 20) that determines the trigger level, is a DC voltage between +0.5V and +2.0V. The LEVEL signal is a DC voltage, generated in the Digital ASIC. Resistor R2309 and capacitors C2312 and C2313 form a lowpass filter, to convert a pulse width modulated signal into the DC voltage.

Delta-T circuit

The Delta-T circuit measures the time between a trigger pulse and the moment the input signal is sampled. Figure 3.14 shows the timing diagram with relation to the signal HLDF (input 10), START (internal), STOPN (output 9), and TOUT (output 15).



START: internal (in the A-ASIC) start signal for the Delta-T measurement.

TOUT: a voltage proportional to the measured value (time) of Delta T.

Figure 3.14 Timing diagram Delta-T circuit

Control logic

The control logic section contains a serial-in parallel-out shift register. This section gets its data from the microprocessor (D1201, circuit diagram A1, figure 10.2) via the CDAT (serial data), CCLK (serial clock), and DTAE (data-latch) lines. The control logic section controls all functional blocks within the A-ASIC.